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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,239	04/16/2004	Ming-Wei Hsu	TOP 369	7782

23995 7590 10/25/2005

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EXAMINER	
BUI, BRYAN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,239	HSU ET AL.	
	Examiner	Art Unit	
	Bryan Bui	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicants' papers filed on 9/21/2005 have been received and entered. Claims 1, 9, 12, 15, 18, 19, 20 have been amended. Claims 1-20 are pending in the application.

2. Applicants' remark has been considered, but it is moot in view of the new ground rejection.

3. The examiner reminds to the Applicant that during patent examination, the pending claims must be given the broadest reasonable interpretation. Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claims, one issued will be interpreted more broadly than is justified. In re prater, 415 F.2d1393, 1404-05, 162 USPQ541, 550-51 (CCPA 1969).

In response to applicant's argument that the reference fails to teach the "outputting of a distinct and separate optimization verification signal" and "transforming the voltage level of the optimization verification signal to a second voltage level", and applicants concludes that "Applicants submitted prior art discloses only generation of a bus connection signal (LDTSTOP# with high voltage level) by transforming the voltage level of the bus disconnection signal, but not transformation of the voltage level of an optimization verification signal" , it is noted that the "Detailed Description Of The Invention" in the current application as specified by applicants in page 9, lines 3-10 and figure 5, steps 30-32 does not mentioned at all about the transformation of the voltage level of **an optimization verification signal, but It is still indicated the LDT bus operates at the optimized bus width and operating frequency set in Bios** as disclosed in the related art (pages 2-4). Further, the explanation which relies to the

specification are not recited in the rejected claim(s), and the extend limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Accordingly, Examiner's position that these limitations are disclosed in the related art submitted by applicants.

Applicants argue that the Habib does not mention of OR logic gate. Examiner's position that Habid discloses the OR logic gate in column 9, lines 15-30.

4. Claim 18 is objected to because of the following informalities: In line 6, one of the duplicates term "signal" should be removed. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' submitted prior art in figures 1-2, and under related art, pages 1-4.

With respect to claim 1, Applicant's submitted prior art (first level voltage and second level voltage are either a high voltage level or low voltage level) discloses all the limitations of the claims which provides a method for verifying optimization of processor link for a system comprising a Northbridge (figure 1, item 14), a bus (figure 1, item 12) coupled between a CPU (figure 1, item 10) and the Northbridge, and a Southbridge (figure 1, item 18), the method comprising the

following steps: setting an initial bus width and an initial bus frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency (page 3, lines 4-15); generating a read request to read the Southbridge (page 3, lines 17-18); output of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request (page 3, lines 19-23), initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level (page 3, lines 16-17); output of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value and transforming the voltage level of the optimization verification signal to a second voltage level (page 2, lines 22-29); and reconnection of the CPU and the Northbridge by the bus according to the bus connection signal, wherein the bus operates at another bus operating bus width and another bus operating frequency (page 2, line 29 to page 3, line 2; page 3, line 28 to page 4, line 2). Applicants' prior art does not mentioned about outputting an optimization verification signal. However, prior art discloses (exactly the same technique shows in **the Detail Description of the current application)** the optimization of LDT I/O bus is achieved through disconnection and reconnection of LDT I/O bus, and the disconnection and reconnection of LDT bus are performed according to the voltage level of the signal LDTSTOP# output by the southbridge (the output voltage level can be considered as a first voltage level (either high or low) in page 2, lines 12-21 and page 3, line 15 to page 4, line

2). Thus, it would have been obvious to one of ordinary skill in the art to realize the outputting optimization signal as claimed is commonly provided in the output of signal LDTSTOP# at the voltage level (corresponding to high level as in example in prior art, page2, line 18-21).

With respect to claims 2-7, Applicant's submitted prior art teaches wherein the bus is a lightning data transport bus (page 1, line 18); wherein the bus is a hyper-transport bus (page 1, line 19); further comprising the step of setting an optimized bus operating bus width and an optimized bus operating frequency of the bus (page 3, lines 12-13); wherein the bus operates at the optimized bus operating bus width and the optimized bus operating frequency when the CPU and the Northbridge are reconnected (page 3, lines 26-30); wherein the bus disconnection signal and the bus connection signal are output by a single output terminal, and wherein the bus disconnection signal and the bus connection signal are generated by asserting and de-asserting a signal output by the Southbridge (page 2, lines 15-29).

With respect to claim 12, Applicant's submitted prior art (first level voltage and second level voltage are either a high voltage level or low voltage level) discloses all the limitations of the claims which provides verifying optimization of processor link for a system comprising a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge, the method comprising the following steps: setting an initial bus width, an initial bus frequency, a bus operating bus width

and a bus operating frequency of the bus coupled between the CPU and the Northbridge (figure 1and figure 2, items S1-S2), wherein the bus operates at the initial bus width and the initial bus frequency and setting an optimized bus operating bus width and an optimized bus operating frequency of the bus (page 3, line 4-15) generating a read request to read the Southbridge; output of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request (page 3, lines 19-23), initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level (page 3, lines 16-17); outputting of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value and transforming the voltage level of the optimization verification signal to a second voltage level (page 2, lines 22-29); and reconnection of the CPU and the Northbridge by the bus according to the bus connection signal, wherein the bus operates at another bus operating bus width and another bus operating frequency (page 2, line 29 to page 3, line 2; page 3, line 28 to page 4, line 2). Applicants' prior art does not mentioned about outputting an optimization verification signal. However, prior art discloses (exactly the same technique shows in **the Detail Description of the current application)** the optimization of LDT I/O bus is achieved through disconnection and reconnection of LDT I/O bus, and the disconnection and reconnection of LDT bus are performed according to the voltage level of the signal LDTSTOP# output by the southbridge (the output voltage level can be considered as a first voltage

level (either high or low) in page 2, lines 12-21 and page 3, line 15 to page 4, line 2). Thus, it would have been obvious to one of ordinary skill in the art to realize the outputting optimization signal as claimed is commonly provided in the output of signal LDTSTOP# at the voltage level (corresponding to high level as in example in prior art, page2, line 18-21).

With respect to claims 13-16, Applicant's submitted prior art teaches wherein the bus is a lightning data transport bus (page 1, line 18); wherein the bus is a hyper-transport bus (page 1, line 19); further comprising the step of setting an optimized bus operating bus width and an optimized bus operating frequency of the bus (page 3, lines 12-13); wherein the bus operates at the optimized bus operating bus width and the optimized bus operating frequency when the CPU and the Northbridge are reconnected (page 3, lines 26-30); wherein the bus disconnection signal and the bus connection signal are output by a single output terminal, and wherein the bus disconnection signal and the bus connection signal are generated by asserting and de-asserting a signal output by the Southbridge (page 2, lines 15-29).

Claims 8-11 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's submitted prior art in figures 1-2, and under the related art, pages 1-4 in view of Habid et al (US 6,903,583).

Applicant's submitted prior art teaches the specific features of the claimed invention that output the optimization verification signal including the signal level (voltage level) output at terminal of the Southbridge; wherein the signal level (voltage level) is coupled to the input terminals of the CPU or the Northbridge as discloses by Applicant's submitted prior art in page 3, lines 7-29, and figure 1, during power management of CPU and Lighting data transport I/O bus between CPU and Nothbridge. Applicants prior art submitted does not mention a signal level detecting circuit. Habid et al teach a signal level detecting circuit comprising a flip-flop and an OR gate logic gate, the flip-flop outputs the optimization verification signal with the first voltage level when the Southbridge outputs the bus disconnection signal, and outputs the optimization verification signal with the second voltage level when the Southbridge outputs the bus connection signal (column 9, lines 15-30); wherein the signal level detection circuit is coupled to the output terminal of the Southbridge; wherein the signal level detection circuit is coupled to the input terminals of the CPU or the Northbridge (figure 2 column 3, line 56 to column 4, line 58, and column 6, lines 14-32). It would have been obvious to one of ordinary skill in the art to modify applicant's submitted prior art to include voltage level detecting circuit comprising a flip-flop and an OR gate logic gate, the flip-flop outputs the optimization verification signal with the first voltage level when the Southbridge outputs the bus disconnection signal, and outputs the optimization verification signal with the second voltage level when the Southbridge outputs the bus connection signal in order to control the voltage signal to optimizing the bus width and operating frequency of Lightning data transport according to level signals.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryan Bui whose telephone number is 571-272-2271. The examiner can normally be reached on M-Th from 7am-4pm, and Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BB

10/24/05

BRYAN BUI
PRIMARY EXAMINER